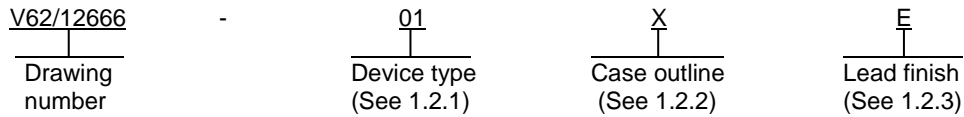


REVISIONS																					
LTR	DESCRIPTION	DATE	APPROVED																		
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PMIC N/A				PREPARED BY RICK OFFICER								DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil/									
Original date of drawing YY-MM-DD 12-12-12				CHECKED BY RAJESH PITHADIA								TITLE MICROCIRCUIT, LINEAR, CMOS, ULTRALOW NOISE, 200 mA, LINEAR REGULATOR, MONOLITHIC SILICON									
				APPROVED BY CHARLES F. SAFFLE																	
				SIZE A		CODE IDENT. NO. 16236						DWG NO. V62/12666									
				REV								PAGE 1 OF 11									

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance CMOS, ultralow noise, 200 mA, linear regulator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:



1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ADP151	CMOS, ultralow noise, 200 mA, linear regulator

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	5	MO-193-AB	Small outline package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

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1.3 Absolute maximum ratings. 1/

Regulator input supply (V_{IN}) to ground (GND)	-0.3 V to +6.5 V
Regulator output voltage (V_{OUT}) to GND	-0.3 V to V_{IN}
Enable input (EN) to GND	-0.3 V to +6.5 V
Storage temperature range (T_{STG})	-65°C to +150°C
Operating junction temperature range (T_J)	-55°C to +125°C

1.4 Recommended operating conditions. 2/

Operating free-air temperature range (T_A)	-55°C to +125°C
Input and output capacitance (C_{MIN})	0.7 μ F 3/
Capacitor equivalent series resistance (R_{ESR})	0.001 Ω to 0.2 Ω

1.5 Thermal characteristics.

Thermal resistance, junction to ambient (θ_{JA})	174°C/W
Thermal resistance, junction to board (θ_{JB})	43°C/W

-
- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.
- 3/ The minimum input and output capacitance should be greater than 0.7 μ F over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

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2. APPLICABLE DOCUMENTS

JEDEC Solid State Technology Association

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

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TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit	
					Min	Max		
Input voltage range	V _{IN}		-55°C to +125°C	01	2.2	5.5	V	
Operating supply current	I _{GND}	I _{OUT} = 0 μA	+25°C	01	10 typical		μA	
			-55°C to +125°C			20		
		I _{OUT} = 100 μA	+25°C		20 typical			
			-55°C to +125°C			40		
		I _{OUT} = 10 mA	+25°C		60 typical			
			-55°C to +125°C			90		
I _{OUT} = 200 mA	+25°C	265 typical						
	-55°C to +125°C		350					
Shutdown current	I _{GND-SD}		+25°C	01	0.2 typical		μA	
			-55°C to +125°C			1.0		
Output voltage accuracy	V _{OUT}	I _{OUT} = 10 mA	+25°C	01	-1	+1	%	
			V _{OUT} < 1.8 V, 100 μA < I _{OUT} < 200 mA, V _{IN} = (V _{OUT} + 0.4 V) to 5.5 V		-55°C to +125°C	-3		+3
					V _{OUT} ≥ 1.8 V, 100 μA < I _{OUT} < 200 mA, V _{IN} = (V _{OUT} + 0.4 V) to 5.5 V	-2.5		+3
Line regulation	ΔV _{OUT} / ΔV _{IN}	V _{IN} = (V _{OUT} + 0.4 V) to 5.5 V	-55°C to +125°C	01	-0.05	+0.05	%/V	
Load regulation <u>3/</u>	ΔV _{OUT} / ΔI _{OUT}	V _{OUT} < 1.8 V, I _{OUT} = 100 μA to 200 mA	+25°C	01	0.006 typical		%mA	
			-55°C to +125°C			0.012		
		V _{OUT} ≥ 1.8 V, I _{OUT} = 100 μA to 200 mA	+25°C		0.003 typical			
			-55°C to +125°C			0.008		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Dropout voltage <u>4/</u>	V _{DROPOUT}	I _{OUT} = 10 mA	+25°C	01	10 typical		mV
			-55°C to +125°C		30		
		I _{OUT} = 200 mA	+25°C		150 typical		
			-55°C to +125°C		230		
Start up time <u>5/</u>	t _{START-UP}	V _{OUT} = 3.3 V	+25°C	01	180 typical		μs
Current limit <u>6/</u> threshold	I _{LIMIT}		0°C to +125°C	01	220	400	mA
Undervoltage lockout input voltage rising	UVLORISE		-55°C to +125°C	01		1.96	V
Undervoltage lockout input voltage falling	UVLO _{FALL}		-55°C to +125°C	01	1.28		V
Undervoltage lockout hysteresis	UVLO _{HYS}		-55°C to +125°C	01	120 typical		mV
Thermal shutdown threshold	T _{SSD}	T _J rising		01	150 typical		°C
Thermal shutdown hysteresis	T _{SSD-HYS}			01	15 typical		°C
Enable (EN) logic high	V _{IH}	2.2 V ≤ V _{IN} ≤ 5.5 V	+25°C	01	1.2		V
Enable (EN) logic low	V _{IL}	2.2 V ≤ V _{IN} ≤ 5.5 V	+25°C	01		0.4	V
Enable (EN) pull down resistance	R _{EN}	V _{IN} = V _{EN} = 5.5 V	+25°C	01	2.6 typical		MΩ
Output noise	OUT _{NOISE}	V _{OUT} = 3.3 V, 10 Hz to 100 kHz, V _{IN} = 5 V	+25°C	01	9 typical		μV rms
		V _{OUT} = 2.5 V, 10 Hz to 100 kHz, V _{IN} = 5 V			9 typical		
		V _{OUT} = 1.1 V, 10 Hz to 100 kHz, V _{IN} = 5 V			9 typical		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits		Unit
					Min	Max	
Power supply rejection ratio	PSRR	V _{IN} = V _{OUT} + 0.5 V, 10 kHz, V _{IN} = 3.8 V, V _{OUT} = 3.3 V, I _{OUT} = 10 mA	+25°C	01	70 typical		dB
		V _{IN} = V _{OUT} + 0.5 V, 100 kHz, V _{IN} = 3.8 V, V _{OUT} = 3.3 V, I _{OUT} = 10 mA			55 typical		
		V _{IN} = V _{OUT} + 1 V, 10 kHz, V _{IN} = 4.3 V, V _{OUT} = 3.3 V, I _{OUT} = 10 mA			70 typical		
		V _{IN} = V _{OUT} + 1 V, 100 kHz, V _{IN} = 4.3 V, V _{OUT} = 3.3 V, I _{OUT} = 10 mA			55 typical		
		V _{IN} = V _{OUT} + 1 V, 10 kHz, V _{IN} = 2.2 V, V _{OUT} = 1.1 V, I _{OUT} = 10 mA			70 typical		
		V _{IN} = V _{OUT} + 1 V, 100 kHz, V _{IN} = 2.2 V, V _{OUT} = 1.1 V, I _{OUT} = 10 mA			55 typical		

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, V_{IN} = (V_{OUT} + 0.4 V) or 2.2 V, whichever is greater; EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 μF, T_A = +25°C.
- 3/ Based on an end point calculation using 0.1 mA and 200 mA loads. See figure 3 for typical load regulation performance for loads less than 1 mA
- 4/ Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.2 V.
- 5/ Start up time is defined as the time between the rising edge of EN and V_{OUT} being at 90% of its nominal value.
- 6/ Current limit threshold is defined as the current at which the output voltage drop to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V (that is 2.7 V).

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Case X

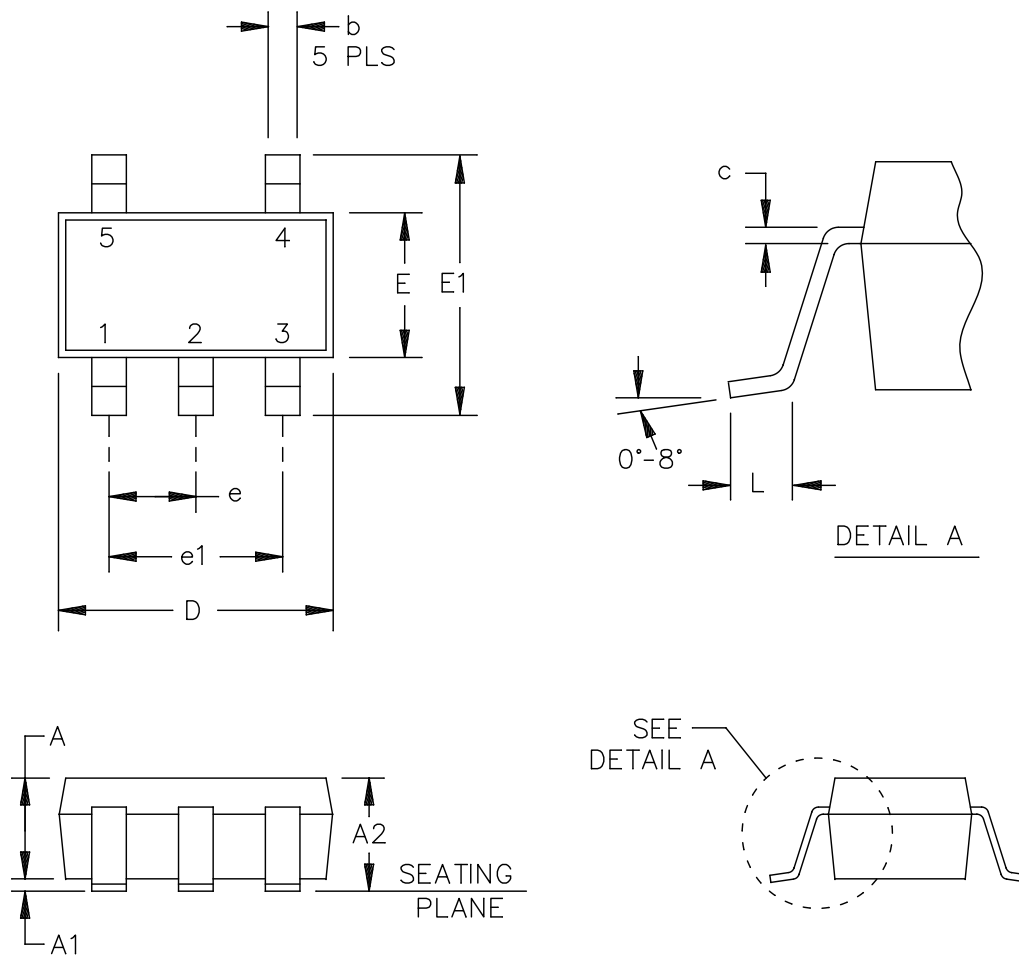


FIGURE 1. Case outline.

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Case X

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.027	.035	0.70	0.90
A1	---	.003	---	0.10
A2	---	.039	---	1.00
b	.011	.019	0.30	0.50
c	.003	.007	0.08	0.20
D	.114 BSC		2.90 BSC	
E	.062 BSC		1.60 BSC	
E1	.110 BSC		2.80 BSC	
e	0.037 BSC		0.95 BSC	
e1	0.074 BSC		1.90 BSC	
L	.011	.023	0.30	0.60

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Falls within reference to JEDEC MO-193-AB with exception of package height and thickness.

FIGURE 1. Case outline - Continued.

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Device type	01	
Case outline	X	
Terminal number	Terminal symbol	Description
1	V _{IN}	Regulator input supply. Bypass V _{IN} to GND with a 1 μF or greater capacitor.
2	GND	Ground.
3	EN	Enable input. Drive EN high to turn on the regulator; derive EN low to turn off the regulator. For automatic startup, connect EN to V _{IN} .
4	NC	No connect. Do not connect this pin.
5	V _{OUT}	Regulated output voltage. Bypass V _{OUT} to GND with a 1 μF or greater capacitor.

FIGURE 2. Terminal connections.

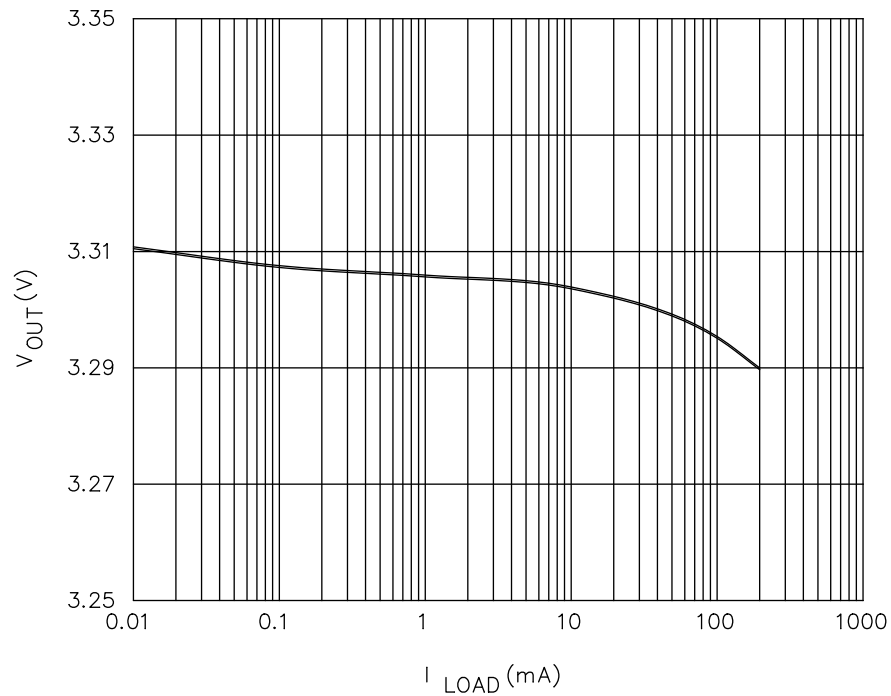


FIGURE 3. Output voltage versus load current.

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4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Vendor part number
V62/12666-01XE	24355	ADP151TUJZ3.3-EPR2

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code

24355

Source of supply

Analog Devices
 Route 1 Industrial Park
 P.O. Box 9106
 Norwood, MA 02062
 Point of contact: Raheen Business Park
 Limerick, Ireland

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